A3 Cont'd

because P2 has a logic state 1 and bit_2 has a logic state 1. Switches S202, S203 are in the open condition because bit_3, bit_4, have a logic state 0. Output switch S204 is in the closed condition, and capacitors C1 and C2 (FIG. 31) of one-bit DACs 162, 164 delivers charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to C*Vref.

In the Claims

Please amend claims 1-3, 7-9, 12, 15-17, 21, 24, 27, 31, 34 and 37-39 as follows:

A4

1. (Amended) A DAC comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

2. (Amended) The DAC of claim 1, wherein the multi-bit digital signal is an equally-weighted multi-bit digital signal, and the associated amount of charge is the same for each of the plurality of sub DACs

3. (Amended) The DAC of claim 1, wherein the multi-bit digital signal is an equally-weighted multi-bit digital signal, and the associated capacitance is the same for each of the plurality of sub DACs.

A5

7. (Amended) The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one

A4 Cont'd

of the at least two of the plurality of switched capacitor cells is angularly offset relative to the orientation direction of at least one other of the at least two of the plurality of switched capacitor cells, the angular offset being substantially, ninety degrees.

8. (Amended) The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has a orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells .

9. (Amended) A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

A5

12. (Amended) A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

A6

15. (Amended) The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset relative to the orientation direction of at least one other of the at least two of the plurality of switched capacitor cells.

A6 cont'd

16. (Amended) The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has an orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells.

17. (Amended) A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

temporarily connecting at least two of the plurality of capacitors to one another to share charge; and

providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

A7

21. (Amended) A method of converting a equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and

generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

A8

24. (Amended) A method of converting an equally weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and

connecting at least two of the plurality of capacitors to one another to share charge.

A9

27. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

means for temporarily connecting at least two of the plurality of capacitors to one another to share charge; and

means for providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

A10

31. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in an equally-weighted multi-bit signal, and

means for generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

A11

34. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in an equally-weighted multi-bit signal, and

means for connecting at least two of the plurality of capacitors to one another to share charge.

A12

37. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share charge ~~with one another~~, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

A12 Cont'd

38. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

39. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

Please add new claims 40-65 as follows:

A13

40. (New) The DAC of claim 1 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

41. (New) The DAC of claim 1 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

42. (New) The DAC of claim 12 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

43. (New) The DAC of claim 12 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

A13 cont'd

44. (New) The method of claim 17 further comprising generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

45. (New). The method of claim 17 wherein connecting comprises connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

46. (New) The method of claim 24 further comprising generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

47. (New) The method of claim 24 wherein connecting comprises connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

48. (New) The DAC of claim 27 further comprising means for generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

49. (New) The DAC of claim 27 wherein means for connecting comprises means for connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

50. (New) The DAC of claim 34 further comprising means for generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

A13 cont'd

51. (New) The DAC of claim 34 wherein means for connecting comprises means for connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

52. (New) The DAC of claim 37 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

53. (New) The DAC of claim 37 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

54. (New) The DAC of claim 39 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

55. (New) The DAC of claim 39 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

56. (New) The DAC of claim 1 wherein the DAC has more than one charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another.

57. (New) The DAC of claim 1 wherein the DAC has more than one operating state, subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

58. (New) A DAC comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an

A13 Cont'd

associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

59. (New) The DAC of claim 58 wherein the DAC has more than one charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another.

60. (New) The DAC of claim 58 wherein the DAC has more than one operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

61. (New) The DAC of claim 58 wherein in the operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal, the sub DACs that are connected to the output terminal deliver charge to said output terminal.

62. (New) A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

connecting at least two of the plurality of capacitors to one another to share charge; and

connecting fewer than all of the plurality of sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal.

A13 concl'd

63. (New) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

means for connecting at least two of the plurality of capacitors to one another to share charge; and

means for connecting fewer than all of the plurality sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal.

Sub B6

64. (New) An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

65. (New) The DAC of claim 15 wherein the angular offset is substantially ninety degrees.

REMARKS

This Amendment is in response to the Office Action mailed on July 12, 2001 objecting to the specification and rejecting all of the claims. The specification has been amended. Claims 1-3, 7-9, 12, 15-17, 21, 24, 27, 31, 34 and 37-39 have been amended. Claims 40-65 have been added. Marked-up versions of the amended specification and the amended claims are attached hereto. Applicants respectfully submit that all of the pending claims are patentable. Accordingly, Applicants respectfully request reconsideration, withdrawal of the objections and rejections, and allowance of all of the claims.